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3	505	(703/13).CCLS.	USPAT	2004/08/26 14:49
4	3	((703/13).CCLS.) and (domino same (circuit or gate or latch))	USPAT	2004/08/26 14:51
5	0	((703/13).CCLS.) and (domino same (circuit or gate or latch))) and erroneous	USPAT	2004/08/26 14:51

L Number	Hits	Search Text	DB	Time stamp
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2	1	("6128769").PN.	USPAT	2004/08/26 16:23
3	1	(wijeratne and sapumal).in.	USPAT; US-PGPUB	2004/08/26 16:35
4	3	(nardin and mark).in.	USPAT; US-PGPUB	2004/08/26 16:37
5	1	("6167642").PN.	USPAT	2004/08/26 16:37

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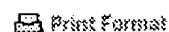
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Pages:266 - 280

[Abstract] [PDF Full-Text (372 KB)] IEEE JNL

**2 Low-speed scan testing of charge-sharing faults for CMOS domino circuits**

*Cheng, C.H.; Jone, W.B.; Chang, S.C.; Wang, J.S.;*  
Electronics Letters, Volume: 36, Issue: 20, 28 Sep 2000  
Pages:1684 - 1685

[Abstract] [PDF Full-Text (252 KB)] IEEE JNL

**3 Low-speed scan testing of charge-sharing faults for CMOS domino circuits**

*Cheng, C.H.; Jone, W.B.; Wang, J.S.; Chang, S.C.;*  
Defect and Fault Tolerance in VLSI Systems, 2000. Proceedings. IEEE International Symposium on, 25-27 Oct. 2000  
Pages:329 - 337

[Abstract] [PDF Full-Text (472 KB)] IEEE CNF

**4 Adaptable voltage scan testing of charge-sharing faults for domino circuits**

*Ching-Hwa Cheng;*  
Defect and Fault Tolerance in VLSI Systems, 2002. DFT 2002. Proceedings. 17th IEEE International Symposium on, 6-8 Nov. 2002  
Pages:147 - 155

[Abstract] [PDF Full-Text (1135 KB)] IEEE CNF

**5 Charge sharing fault detection for CMOS domino logic circuits**

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Defect and Fault Tolerance in VLSI Systems, 1999. DFT '99. International Symposium  
on , 1-3 Nov. 1999  
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